CMC203 FERA Driver / Memory / Histogrammer

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The CMC203 FERA driver / memory / histogrammer is designed to be a compatible replacement and upgrade for the LeCroy model 4301 FERA driver. All signals and connectors are compatible with the 4301. The FERA output ECLbus is at the rear of the module, all other connections are on the front panel.

There are five basic modes of operation:

- As a plain 4301 FERA driver. ECL in and ECL out, no buffering. This mode is a drop in replacement for a LeCroy 4301 and is the default mode on power up. All other modes are selected using CAMAC commands

- As an enhanced 4301, ECL in and ECL out. With a 2k FIFO buffer, input and output handshakes (wst/wak) are independent and de-coupled. This works well with a simple memory module as the destination.

- As an enhanced 4301, ECL in and ECL out. With a 2k FIFO buffer and the addition of an external ren/pass. This allows another FERA driver to be the data destination, and allows concatenation of multiple FERA data streams.

- As a FERA driver and memory combination. ECL in and CAMAC dataway readout, with a 1 Mword (1,048,576) FIFO buffer between FERA in and CAMAC out. CAMAC read and FERA input can proceed simultaneously.

- As a FERA driver and histogram memory combination. ECL in and CAMAC readout of the histogram array. The 1 Mword memory is used for histogram storage.

The following features are available in all modes, even the plain 4301 mode. All adjustments and selections are made with CAMAC registers:

12 bit DAC output, 0 to 10.2375 Volts, ?1/2 lsb over full range.
The FERA request delay is adjustable from 400 nS to 160 microseconds, in 40 nS steps
Optional pass input to close ren/pass loop
Optional send Clear pulse, width adjustable up to 160 microseconds, 40 nS steps,
Optional send GATE pulse, width adjustable up to 40 microseconds, 10 nS steps
Optional BUSY output (from gate or request input to end of event)
Optional gate timeout, if gate but no request, adjustable up to 160 microseconds
Optional event timeout, if request, but no end of event, adjustable up to to 2.4 milliseconds
Optional clear after event readout
Optional delay after clear before end of event (end of BUSY)
Seven 48 bit counters for gates, requests, clears, headers, timeouts and histogram count.

In the FIFO modes, special headers can be inserted in the data stream when gates, requests, clears or time outs occur. In the 1Mword FIFO mode, a Lam is set when the FIFO becomes half full.

In the histogram mode, there is a choice of 16 bit (65k max) or 32 bit (4G max) histogram elements, with corresponding 20 bit or 19 bit address space. The vsn from the header can be concatenated with the data to histogram many modules at once, or a register can be used to select the histogram base address, allowing multiple, time dependent histograms of a 15 bit address space. The readout block size is set by a register to ease readout of histograms with less than 15 bit address spaces. A 48 bit counter records the total number of hits contained in the histogram(s).

FASTCAMAC level 1 readout (400 nS/word) is available in FIFO memory and histogram modes. The module is ready for level 2, requiring only a firmware upgrade when level 2 crate controllers become available.

All control logic in the CMC203 is contained in five programmable logic devices. The firmware is readily modified to meet unforeseen requirements or special applications. Firmware upgrades, when available, will be performed at no charge if the module is returned to the factory. The upgrade can be done in the field, if necessary.

CAMAC Commands (ordered by Function code and subAddress)

F & A	*command*	*description*
F0 A0	Readdac	read 12 bit dac (register is 24 bits, r/w)
F0 A1	Readcsr	read control register
F0 A2	Readreqd	read request delay register
F0 A3	Readgatw	read test gate width register
F0 A4	Readclrw	read FERA clear width register
F0 A5	Readblks	read histogram readout block size register
F0 A6	Readmult	read multi histogram address register
F0 A7	Readgto	read gate time out
F0 A8	Readbdl	read busy end delay
F0 A9	Readvsn	read 8 bit vsn for special headers and trailers
F0 A10	Readvn	read FPGA firmware version number
F0 A11	Readpp	read ping-pong register
F0 A12	Readleds	read led selection register
F0 A13	Readext	read external output selection register
F0 A14	Readeto	read event time out register
F0 A15	Readexin	read external input selection register
F1 A0	rdmemry	read memory at address counter, increment address
F1 A1	Readaddr	read address counter
F1 A2	Rdmnobmp	read memory at address counter, no increment
F2 A0	ReadFIFO	read next word from FIFO, Q=0 when empty
F2 A1	RdFIFOcount	read number of words in FIFO
F2 A2	Readgatcnt	read number of gates since last reset, ls 24 bits
F2 A3	Readgatcnta	read number of gates since last reset, ms 24 bits
F2 A4	Readreqcnt	read number of FERA requests since last reset, ls 24 bits
F2 A5	Readreqcnta	read number of FERA requests since reset, ms 24 bits
F2 A6	Readclrcnt	read number of FERA clears since last reset, ls 24 bits
F2 A7	Readclrcnta	read number of FERA clears since last reset, ms 24 bits
F2 A8	Readhdrcnt	read number of FERA headers since last reset, ls 24 bits
F2 A9	Readhdrcnta	read number of FERA headers since last reset, ms 24 bits
F2 A10	Readhstcnt	read number of hits in the histogram array, ls 24 bits
F2 A11	Readhstcnta	read number of hits in the histogram array, ms 24 bits
F2 A12	Readevtto	read number of event timeouts, ls 24 bits
F2 A13	Readevttoa	read number of event timeouts, ms 24 bits
F2 A14	Readgateto	read number of gate timeouts, ls 24 bits
F2 A15	Readgatetoa	read number of gate timeouts, ms 24 bits
F5 A0	FASTrdhist	FASTCAMAC level 1 read of histogram memory
F5 A1	FASTrdFIFO	FASTCAMAC level 1 read of FIFO memory
F8 A0	Testlam	test lam (set when FIFO becomes half full)
F9 A0	F9fbclr	send FERA bus clear (width from width register)
F9 A1	F9data	reset data FIFO and counters
F9 A2	F9hist	reset histogram data (this takes 200 ms)
F9 A3	F9addr	reset address counter to zero
F9 A4	F9all	reset everything, like C or Z
F10 A0	Clearlam	clear lam
F16 A0	Writedac	write 12 bit DAC, 0 to 10.2375 V

F16 A1	Writecsr	write control register
F16 A2	Writereqd	write request delay register, 40 nS lsb
F16 A3	Writegatw	write test gate width register, 10 nS lsb
F16 A4	Writeclrw	write FERA clear width register, 40 nS lsb
F16 A5	Writerblks	write histogram readout block size register
F16 A6	Writemult	write multi histogram register
F16 A7	Writegto	write gate timeout register, 40 nS lsb
F16 A8	Writebdl	write busy end delay register, 40 nS lsb
F16 A9	Writevsn	write 12 bit VSN for header & trailer
F16 A11	Writepp	write ping-pong register, 40 nS lsb
F16 A12	Writeleds	write led selection register
F16 A13	Writextout	write external output selection register
F16 A14	Writeeto	write event time out register, 640 nS lsb
F16 A15	Writeextin	write external input register
F17 A0	Writemem	write memory at address counter
F17 A1	Writeaddr	write memory address counter
F24 A0	Disalam	disable lam
F24 A1	Disa0	disable (both modes)
F24 A2	Disa1	disable (both modes)
F26 A0	Enablam	enable lam
F26 A1	Enab0	enable0 on, honors CAMAC inhibit
F26 A2	Enab1	enable1 on, ignores CAMAC inhibit
F25 A0	Sendtestgate	send gate to FERA control bus, width from width register
F25 A1	Incrmemaddr	increment memory address counter
F27 A0	Tstmerase	test memory erase in progress
F30		Enter special mode to program the FPGAs

Detailed REGISTER Descriptions

DAC register, F16A0, 12 bit value for test DAC output, 0 to 10.2375 volts. This register is 24 bits, r/w

CONTROL register, F16A1, a 12 bit register to select operating mode and other features. Bit 0 is the lsb, bit 11 the msb.

Bit(s)		*value*	*Meaning*
0-2	000	0	4301 emulation mode, this is power up default mode
0-2	001	1	modified 4301, with 2k FIFO
0-2	010	2	modified 4301, with 2k FIFO, with external ren/pass
0-2	011	3	1M FIFO mode, CAMAC readout
0-2	100	4	16 bit histograms
0-2	101	5	32 bit histograms
0-2	110	6	16 bit multi-histogram
0-2	111	7	32 bit multi-histogram
3		8	REN mode 0= normal, 1= pass mode
4		16	send clear at end of event
5		32	not used
6		64	not used
7		128	end busy after clear, else end after ren
8		256	Insert gate header in data stream
9		512	insert request header in data stream
10		1024	insert clear header in data stream
11	msb	2048	not used

Operating modes, CSR Bits 0-2

0 power up as a LeCroy 4301 (logically identical, possible timing differences)

1 4301 with a 2k word FIFO buffer between input and output

2 4301 with a 2k word FIFO buffer and external ren/pass.

3 FIFO mode directs all data to a 1M word FIFO, read by CAMAC

Histogram modes, either 16 bit or 32 bit width, and single or multiple (time dependent).

4,5 16 bit single mode uses the lower 5 bits of vsn (from the header) and 15 bits of data as the histogram address. 32 bit single mode uses only 4 bits from the vsn

6,7 multi mode uses 5 (16 bit mode) or 4 (32 bit mode) bits of the multi register and 15 bits of the data word as the histogram address

REN/PASS mode, CSR bit 3

normal REN (Readout Enable, REO output on front panel) mode ends REN when REQ input ends. pass mode ends REN only when PASS input (PSI input on front panel) is received

Send Clear at end of event, CSR bit 4

If set, send clear when readout is complete
Event ends when: REQ ends, PASS (PSI) returns, or when gate timeout ends (if no request)

Select end of BUSY, CSR bit 7. BUSY begins when GATE or REQUEST arrives.

0= End BUSY when Readout Enable (REO) ends
1= End BUSY after end of CLEAR.
If end of busy delay register is non-zero, also wait untilend of delay (delay starts at end of REO or end of CLEAR).

Insert special gate header in data stream, CSR bit 8.
gate header format = 11000VVVVVVVVVVV, inserted when GATE detected
V is the VSN from the register at F16A9

Insert special request header in data stream, CSR bit 9.
request header format = 11100VVVVVVVVVVV, inserted when REQ detected
V is the VSN from the register at F16A9.

Insert special clear header in data stream, CSR bit 10.
clear header format = 11111CCCCVVVVVVV, inserted at beginning of CLEAR
V is the VSN from the register at F16A9, C identifies the reason for the clear.

CCCC	*the source of the clear.*
0000	clear at the end of a normal event, when REO is deasserted.
0001	external clear input
0010	clear from F9A0 command
0011	clear from gate time out
0100	clear from event time out

REQUEST DELAY register, F16A2, 12 bits, 40 ns resolution (160 microseconds max)
this is the delay between req (in) and reo (out), default (when register value=0) is 400 nS.

TEST GATE WIDTH register, F16A3, 12 bits, 10 ns resolution (40 microseconds max)

FERA CLEAR WIDTH register, F16A4, 12 bits, 40 ns resolution (160 microseconds max)
default (when register value=0) is 200 nS.

HISTOGRAM READOUT BLOCK SIZE register, F16A5, default = 1M (all of memory)

MULTI HISTOGRAM register, F16A6, bits 15-19 of histogram address

GATE TIME OUT register, F16A7, 12 bits, 40 ns resolution (160 microseconds max)
default is zero, no time out. The time out value must be set longer than the maximum delay expected between the gate and the req. the req cancels the time out.

BUSY END DELAY register, F16A8, 12 bits, 40 ns resolution (160 microseconds max)
default is zero delay, BUSY ends at end of CLEAR.

VSN register, F16A9, ID number (VSN) in the special headers inserted by FERA driver

PING PONG INTERVAL register, F16A11, 12 bits, 40 ns resolution (160 microseconds max)

LED ASSIGNMENT register, F16A12

This register controls the behavior of the two leds (light emitting diodes) on the front panel. Bits 0-5 control LED A, bits 6-11 control LED B

LED A defaults to full, LED B defaults to BUSY

value	*Led A (0-5)*	*Led B (6-11)*	*Description*
000000	Full	Busy	
000001	Enable	Enable	
000010	Busy	Busy	
000011	Busreq	Busreq	
000100	Buswst	Buswst	
000101	Buswak	Buswak	
000110	Extwst	Extwst	
000111	Extwak	Extwak	
001000	Ren	Ren	
001001	Psi	Psi	
001010	Full	Full	(FIFO is full)
001011	LAM	LAM	
001100	Empty	Empty	(FIFO is empty)
001101	Fifo14	Fifo14	(1M FIFO is 1/4 full)
001110	Fifo12	Fifo12	(1M FIFO is 1/2 full)
001111	Fifo34	Fifo34	(1M FIFO is 3/4 full)

EXTERNAL OUTPUT SELECTION register, F16A13

There are four external outputs on the front panel, two ECL differential pairs (labeled wso & rqo) and two NIM coaxial (labeled S & Q). This 12 bit register controls which internal signals are routed to these outputs. When the corresponding register bits are “000”, the output defaults to the same as the LeCroy 4301.

lsb											
0	1	2	3	4	5	6	7	8	9	10	11
WSO			RQO			S			Q		

value	*Output WSO*	*Output RQO*	*Output S*	*Output Q*
000	wso	Request	wso	request
001	request	Wso	request	wso
010	extpass	Extpass	extpass	extpass
011	ppout1	Ppout2	ppout1	ppout2
100	foinpr	Foinpr	foinpr	foinpr
101	begfo	Begfo	begfo	begfo
110	endfo	Endfo	endfo	endfo
111	busy	Busy	busy	busy

bits 0-2 controls ECL WSO, default external write strobe
bits 5-3 controls ECL RQO, default external request
bits 8-6 controls NIM S default external write strobe
bits 11-9 controls NIM Q default external request

ppout1 & ppout2 are an alternating pair of pulses, spaced by the value in the ping-pong register

begfo (begin FERA out) and endfo (end FERA out) are a pair of pulses indicating the beginning and end of the event to an external receiver for the FERA output data. foinpr (FERA out in progress) begins at begfo and ends at endfo.

EVENT TIME OUT register, F16A14, 12 bits, 640 nS resolution (2.4 milliseconds max)

the default is zero, no time out. The time out value must be set longer than the maximum delay expected between the gate and the end of the event

EXTERNAL REN (EXTREN) INPUT SIGNAL SELECT register, F16A15.

In mode 2, an input port is required for the external REN signal. This register selects from among the available ports an input to use for this signal. Only one should be selected.

value	*Port used for REN*
1	ecl clear
2	ecl readinh
4	ecl wak
8	ecl psi
16	nim clear
32	nim readinh
64	nim wak

Control Commands

F9 clear modes:

A0 sends clear on FERA control bus, width from register, default 1 microsecond
A1 clears all data, FIFO and counters, not registers
A2 resets the histogram memory to zero. this takes 200milliseconds. test with f27,a0
A3 resets the memory readout address counter to zero
A4 resets everything (except histogram memory), same as C or Z

Sendtestgate, F25A0, sends a gate to the FERA control bus, whose width is determined by the gate width register. Width range from 10 nS to 40.95 microseconds, in 10 nS steps

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Read Commands

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readFIFO, F2A0, reads next word from the FIFO, Q=0 when empty (invalid data). read any time.

read memory, F1A0.

this register uses the address counter.
Q= 0 when readout block size is exceeded. This is useful when the data words are less than 15 bits (smaller histograms). Just reload the address counter to the beginning of the next histogram and continue reading.

There are seven 48 bit counters, read as two 24 bit read commands

F2A2,A3	gates sent to FERAbus
F2A4,A5	requests received from FERABus
F2A6,A7	clears sent to FERABus
F2A8,A9	headers read in from FERABus,
F2A10,A11	total histogram hits recorded.
F2A12,A13	event timeouts
F2A14,A15	gate timeouts

Notes

The Clear Commands

There are five different F9 commands, A0-A4. These allow selective clearing of the module, and the modules on the FERAbus.
F9A0 just sends a CLEAR on the FERAbus. The width is determined by the width register (F16A4).
F9A1 resets all FIFOs and all of the 48 bit counters
F9A2 clears the histogram memory by setting each element to zero. This is a sequential operation, and takes about 200 milliseconds. Use F27A0 to determine when the clearing is complete.
F9A3 resets the memory address counter to zero.
F9A4 clears and disables everything (except for clearing the histogram memory). This is equivalent to a CAMAC Z or C command.

The Enable and Disable commands

There are three enable/disable pairs (F26/F24), A0-A2.
F26A0 enables the LAM
F26A1 and F26A2 enable the detection of Gates, Requests and Clears. When disabled, no REO will ever be output. This effectively stops all operating modes of the CMC203 except the basic 4301 mode (which does mot require an enable). The difference between the two commands is the treatment on CAMAC Inhibit (the I line on the CAMAC dataway). F26A1 honors the inhibit.signal. Inhibit will disable the module as if an F24A1 or F24A2 command had been received. F26A2 ignores the inhibit signal.
While disabled, the BUSY output (one of the optional output signals) is TRUE. The histogram memory can be safely read when the module is disabled.
Enable and Disable also control the ping-pong pulse generation.

The DAC output on the FERAbus

This is a high quality 12 bit DAC with integral and differential linearity of ½ lsb. During final test, the endpoints are trimmed to be within ½ lsb. This is provided for compatibility with the original LeCroy 4301, and was used to calibrate the 4300b adc modules.

The FERA Request delay

The delay between the receipt of a Request from the FERAbus and the assertion of REO is adjustable using the 12 bit register at F16A2. The minimum delay (when the register is zero) is about 400 nSec. It can be adjusted in steps of 40 nSec up to 160 microseconds. This is used to ensure that all modules on the FERAbus are ready before REO is asserted.

The PSI (PASS input) signal

This is an optional method to signal to the CMC203 that the FERA read is complete. If bit 3 (value = 8) of the CSR (F16A1) is zero, the end of the Request signal determines the end of the REO. If bit 3 is one, the REO will continue to be asserted until the PASS signal (from the last module on the FERAbus) is returned via PSI.

Sending a CLEAR pulse with a CAMAC command

The F9A0 command sends a CLEAR on the FERAbus. The width is determined by the width register (F16A4).

Sending a TESTGATE pulse with a CAMAC command

The F25A0 command sends a GATE pulse to the FERAbus. The width is determined by the 12 bit register at F16A3. The width can be as short as 10 nSec, maximum 40 microseconds, in 10 nSec steps. This test GATE is OR'ed with the other two GATE sources, the NIM input (G) and the ECL input (GATE).

The BUSY output signal

This is an internal signal that indicates an event in progress. It begins with the detection of either a GATE or REQUEST signal. BUSY can drive an external output and/or an LED, by appropriately setting the external output selection register (F16A13) and the led selection register (F16A12). BUSY can also be used as part of the trigger system that generates the GATE, and can prevent spurious gates when the system is not ready to accept them.
The end of the BUSY occurs at the end of REQUEST, the end of CLEAR or after the BUSY end delay, depending on the register settings.
Note that an event can begin with just a REQUEST. A GATE on the FERAbus is not required by the CMC203.

The GATE time out

The gate time out register (F16A7) determines how long to wait, after a GATE is detected, for a REQUEST to be detected. The wait can be set from 40 nSec to 160 nSec, in 40 nSec steps. A value of zero disables this feature. This is useful for situations in which a GATE does not always produce data to read out (and the corresponding Request signal). Any time outs that occur are counted, and the number can be read over CAMAC (F2A14, F2A15). The gate time out always triggers a Clear, independent of bit 4 of the control register. If the clear special header is enabled, the

The EVENT time out

The event time out register (F16A14) determines how long to wait for the end of the event, after BUSY is asserted. The wait can be from 640 nSec to 2.4 milliseconds, in 640 nSec steps. A value of zero disables this feature. This is useful to prevent system hang-ups due to FERAbus handshake errors. Any time outs that occur are counted, and the number can be read over CAMAC (F2A12, F2A13).). The event time out always triggers a Clear, independent of bit 4 of the control register. Use this feature with care. The time out should be long enough to cover all expected processing and readout delays

Sending a CLEAR at the end of the event

If bit 4 (value = 16) of the control register is set to '1', then a Clear is sent on the FERAbus at the end of the event when REO ends). The width is determined by the clear width register *F16A4).

The BUSY end delay

This register (F16A8) determines how long after the end of CLEAR the BUSY signal continues to be asserted. The delay can range from 40 nSec to 160 microseconds, in 40 nSec steps. A value of zero, disables this feature. This delay can be used to provide extra time after the end of the Clear pulse for complete recovery of an ADC module.

Ping-Pong pulses

Ppout1 and Ppout2 are an alternating pair of pulses, each 40 nSec long. The interval between them is set by the ping-pong register, F16A11. The interval can be set from 40 nSec to 160 microseconds, in 40 nSec steps. The total period then ranges from 80 nSec to 320 microseconds. The outputs used by these pulses are determined by the external output selection register (F16A13). These pulses are intended to provide alternating COM pulses to a pair of 3377 TDCs to produce a very long range TDC.

Inserting Special Headers in the data stream

In all modes except the plain 4301 mode, special headers can be inserted in the data stream. These will all have the msb set to 1, to distinguish them from data (but not from headers read in from the FERAbus). The next 3 bits identify the event that prompted the insertion of the header. If the event was a clear the next 4 bits identify the source. The remaining bits are taken from the VSN register, F16A9. The VSN should be unique, to allow easy identification of these headers.

These special headers are intended as a diagnostic aid, when setting up a FERA system, or when experiencing difficulty. They should normally be disabled.

OPERATING THE CMC203

Powering up the CMC203

All control logic in the CMC203 is contained in five programmable logic devices, 3 CPLDs and 2 FPGAs. The CPLDs are non-volatile, and are programmed during assembly. The FPGAs are memory based and are loaded automatically on power up from a read only memory. The normal operation is that the two leds (A&B, the N led will not illuminate) will both illuminate for about 0.5 S, and then led A turns off, leaving B on. This indicates that the FPGAs have been successfully loaded. The first command after the FPGA's are loaded should be an F9 command, any subaddress. This ensures that the boot loader is disabled.

With some CAMAC crates and crate controllers, the automatic load on power up fails, and the firmware must be loaded by CAMAC commands. This is indicated by the two leds (A&B) remaining illuminated. This problem is being investigated. If your CAMAC crate is in this situation, you should force the loading of the FPGAs during your initialization. The following sequence of CAMAC commands sent to the module will load the FPGAs. These commands are interpreted by the CPLD that controls the loading of the FPGAs. The subaddress is not decoded, so any subaddress will work. The F30 command enables decoding of the F25 command. After the final F9 command these commands are disabled, except for the F30 command, which allows reloading of the FPGAs at any time.

F9
F30
F25 The A led will go out after about 0.5 S.
Then send an F9 to disable the f25 and put the module into the default (4301) mode

The firmware in the CMC203 is readily modified to meet unforeseen requirements or special applications. Firmware upgrades, when available, will be performed at no charge if the module is returned to the factory. The upgrade can be done in the field, if necessary, by using special software. The firmware version number can be read with F0A10.

The plain 4301 emulation mode

This is the default mode on power up, and after a CAMAC Z, C or F9A4 command. Note that most of the optional features can be used in this mode by setting the appropriate register.

There are some minor differences between this mode and a LeCroy 4301.

All FERA signals (except the Gate) pass through an FPGA. The transit delays through the module are longer than the LeCroy 4301 (which is typically about 4 nSec). This mode will be slower than a LeCroy 4301.

The Clear inputs (ECL and NIM) are detected on the leading edge and trigger a clear pulse on the FERA bus. The width of the input signal is not relevant. The width of the Clear output is determined by the clear width register (F16A4). The default width (when the register set to zero) is 200 nanoseconds.

The minimum Request delay is about 400 nSec. The LeCroy 4301 is about 150 nSec.

The CMC203 Modes

All modes except the plain 4301 mode utilize a 100 MHz state machine to read the data from the FERAbus and control the wst/wak handshake. The handshake delays are less than 40 nSec. The data is transferred to a high speed FIFO memory, which de-couples the input from all subsequent processing. If the FIFO is full, the input state machine will pause.

The enhanced 4301 modes

There are two enhanced modes, mode 1 and mode 2. Both modes utilize a 2048 word FIFO between the FERA input and the FERA output. This de-couples the input and output and can allow the readout (to another module via the FERA output bus) to proceed in the background, and not contribute to the dead time.

Mode 1 provides separate and independent WST/WAK handshakes for the FERA input (the FERAbus) and the FERA output (on the rear panel). The readout through the FERA output on the rear panel is de-coupled from the FERA input by the FIFO. If the event data completely fits in the FIFO, the readout can occur after the event has completed.

Mode 2 includes mode 1, and adds an external ren/pass using optional external inputs and outputs. The ren output is selected with the external output register (F16A13), the pass input is selected with the external input register (F16A15). This mode allows multiple CMC203's to be combined into one FERA output data stream. Output bus arbitration is provided by the external ren/pass pair. Combining FERA data streams is best accomplished with ECL logic OR circuits. Wired OR connections are not recommended unless all modules are in the same crate

The One Million Word FIFO mode

In this mode the 1 Mword memory is used as a FIFO. Everything read from the FERAbus and any special headers selected, are stored in the FIFO memory. The data in the FIFO can be read only over CAMAC (not the FERA output bus). The number of words stored in the FIFO can be read at any time with F2A1. When the FIFO becomes half full, a LAM is set (if enabled). Note that the LAM is set *only* when the FIFO *becomes* half full. If the LAM is cleared (F10A0), it will stay cleared until the FIFO contents falls below half and then becomes half full.
The FIFO is read with F2A0 and returns Q=1 for each valid read. When the FIFO is empty, F2A0 returns Q=0.
The FIFO can also be read with FASTCAMAC level 1 (F5A1), if your crate controller supports it. The FASTCAMAC transfer rate is one word every 400 nSec.
The FIFO can be read simultaneously with FERA input. It is not necessary to stop the data acquisition to read out the FIFO. If the FIFO fills up, the FERAbus data input will pause until space is available.

The Histogram modes

These are the most complex modes to program and to read out. There are two basic histogram choices. The first is a single histogram that uses the entire memory space to histogram many modules and channels simultaneously (modes 4&5). The second is a multiple histogram mode. This is a smaller histogram (modes 6&7) that is limited to one module, but can be located in memory to allow recording a time dependent set of histograms (multiple histograms of the same module). The histograms are stored in a static ram memory. The only way to erase this memory is to write zero into each memory element. This is accomplished automatically with F9A2. Test for completion with F27A0, until Q=0. The memory erase operation takes 200 milliseconds.

Each of these modes can be configured for either 16 bit (single word) or 32 bit (double word) histogram elements, making four distinct histogram modes. The 16 bit modes can contain up to 65,535 hits in each element, and have a 20 bit address space (1M elements). The 32 bit modes can contain 4,294,967,295 hits in each element and have a 19 bit address space (512k elements). The count will not wrap around if the maximum is exceeded. The count will remain at the maximum. Any extra hits will still be counted in the 48 bit histogram counter, however. This counter (F2A10&A11) will contain the integral of the complete histogram.

In the single histogram mode, the address of the histogram element is determined by concatenating the 15 data bits in the data word with additional bits taken from the most recent header word (that was read from the FERAbus). Either 5 or 4 bits (16 or 32 bit mode) are taken from the lower order bits of the header and used as the high order bits of the address, creating a 20 or 19 bit address. These added bits are usually part of the 8 bit vsn for the module, and have been set when the module was initialized. By carefully setting the vsn for each module, the histograms for each module) can be placed as desired within the total histogram space.

As an example, consider a crate with 16 LeCroy 4300b ADC modules, each with 16 channels, in 11 bit mode, and with zero suppression enabled. Then each data word consists of 11 bits of data and 4 bits of channel address, for a total of 15 bits. The first module should have the vsn set to zero, the second to 1, etc., up to 15 for the sixteenth module. Using single histogram mode with 32 bit elements, the entire histogram array (256 channels, 2048 double word elements each) will occupy 1,048,576 memory locations (the entire memory). In 16 bit mode, 512 channels (32 4300b modules, more than a full crate!) can be simultaneously histogrammed.

In the multiple histogram mode the 15 data bits in the data word are concatenated with bits taken from the multi-histogram register (F16A6). The header words are ignored. In single word mode the low order 5 bits from the multi-histogram register become the high order bits of the 20 bit memory address. In the double word mode only 4 bits are used. The total memory space will accommodate 16 histograms in double word mode and 32 in single word mode. A new value can be written to the multi-histogram register at any time. The histogramming will immediately move to the new location within the memory space.

As an example, consider a crate with only one 4300b module, initialized as above (11 bits, zero suppression), 16 bit multi-histogram mode. The vsn in the 4300b can be set to any value, it is not used. For the first histogram, set the multi-histogram register to zero. After one minute, change the multi-histogram register to 1, to 2 after another minute, etc. Keep this up for 32 minutes, then disable and read out all 1,048,576 histogram

elements. The result will be a record over 32 minutes, in one minute steps, of the amplitude spectrum for each of 16 detectors, taken simultaneously.

The histogram array is read only over CAMAC. The CMC203 must be disabled (F24A1 or F24A2) before reading the histogram memory array. The block size register defaults to the entire memory. To read the entire memory, just reset the address counter and read with F1A0 1,048,576 times! Reading the entire memory is usually not appropriate, since there will often be large unused stretches of memory. To read out a small section of memory (where the histogram of interest is located) use the following recipe

Load the memory address counter (F17A1) with the first location of the histogram.
(or reset the address counter to zero with F9A3 for the very first histogram)
Load the block size register with the number of words in the histogram.
Read with F1A0 or F5A0 (FASTCAMAC) until no Q?

Repeat this recipe until all histograms are read.

Starting and Stopping the CMC203

The CMC203 is disabled on power up and after a Z, C, or F9A4 command. When disabled, Gates, Requests, and Clears are simply ignored, and the internal BUSY signal is asserted. The Gate is not blocked, incoming Gates are output on the FERA control bus. There are two different enable commands, F26A1 and F26A2. The first (A1) honors the CAMAC Inhibit line on the dataway. The CMC203 will be enabled only if Inhibit is not asserted. The second (A2) ignores the Inhibit signal. The disable commands are F24A1 and F24A2, and are equivalent. Both will disable the CMC203 regardless of which command was used to enable it. The actual disable will not take place if an event is in progress, but will be delayed until BUSY is no longer asserted. When the CMC203 is enabled, Gates, Requests and Clears are detected. Gates cause a special header in the data stream (if enabled), start the Gate Time Out (if set to non-zero), and are counted by the Gate counter. Requests cause a special header in the data stream (if enabled), start the Request Time Out (if set to non-zero), are counted by the Request counter and cause (after the Request Delay) REO to be asserted. Clears cause a special header in the data stream (if enabled), and are counted by the Clear counter.

If the trigger system that supplies the Gate has a veto (or blocking) input, the BUSY should be output on an unused output (see the external output selection register (F16A13) and supplied to the veto input. The trigger will then be blocked whenever the CMC203 is busy reading from the FERAbus, or is disabled. The system can then be started and stopped with the enable/disable commands. This is the best way to operate the CMC203. There are no side effects.

If the trigger is free running, starting and stopping as above may have side effects which may put undesired data into the data stream.

If neither the trigger nor the acquisition modules (the FERA adcs, for example) can be disabled, one solution is to use the Gate Time Out to start and stop. During initialization, set the Gate Time Out to be very short, less than the minimum delay between the beginning of the Gate and the beginning of Request. Then when the CMC203 is enabled, the events will be cleared before the FERA module can send Request, and no events will be read in from the FERAbus. However, Gates and Clears will be counted, and header generated (if selected). When ready to start, clear the counters (and FIFO) with F9A1, and set the Gate Time Out to a value longer than the maximum delay between the Gate and Request. Now events will be properly recognized and recorded. The counters for the Gates and The Clears may be incorrect (and there may be extra special headers) because of the delay between clearing and changing the Gate Time Out, but everything else will be correct. To stop, set the Gate Time Out back to the short value (as before the start).

If the FERA modules can be disabled, but the trigger is free running, that can be used to start and stop. Enable the CMC203, then enable the FERA modules. To stop, disable the FERA modules first, then the CMC203. As in the previous case, the counters may be incorrect and there may be extra special headers, but the data from the FERA modules will be correct.

INPUT AND OUTPUT SIGNALS:

LED Indicators

N, Red, indicates CAMAC dataway operation
A, Yellow, programmable, default is FIFO Full
B, Green, programmable, default is BUSY

FERA control bus, 8 pair connector, all outputs are differential ECL, inputs are single ended ECL

pin	*Name*	*direction*	*Description*
1,2		ground	both pins connect to ground
3,4	WST	input	write strobe from modules on FERAbus
5,6	REQ	input	Request from modules on FERAbus
7,8	CLR	output	Clear pulse to modules on FERAbus
9,10	GATE	output	Gate to modules on FERAbus
11,12	WAK	output	write acknowledge to modules on FERAbus
13,14	GND	ground	both pins connect to ground
15,16	DAC	analog	Pin 15 DAC voltage output, pin 16 ground

FERA auxiliary signals, 8 pair connector, all differential ECL

pin	*Name*	*direction*	*Description*
1,2	CLR	input	External Clear input
3,4	GATE	input	External Gate input
5,6	RINH	input	External read inhibit input
7,8	WAK	input	External write acknowledge input
9,10	WSO	output	External write strobe output
11,12	RQO	output	External Request output
13,14	REO	output	Read enable to first module on FERAbus
15,16	PSI	input	Pass input from last module on FERAbus

LEMO connectors, NIM fast signal levels, 50 ohm impedance

Name	*direction*	*description*
G	input	External Gate input
C	input	External Clear input
I	input	External read inhibit input
A	input	External write acknowledge input
Q	output	External Request output
S	output	External write strobe output

FERA data bus input, 34 pin header, single ended ECL

Lsb on pin1, msb on pin 31
Terminated with 60 ohms to –2V.
Pins 33 and 34 connected to ground through 1k ohm resistors

FERA data bus output, 34 pin header, differential ECL, *ON REAR PANEL*

Lsb on pins1 and 2, msb on pins 31 and 32
390 ohm pull downs to –5.2V (these can be removed, but they are not socketed)
Pins 33 and 34 connected to ground through 1k ohm resistors

Note that differential ECL signals are ‘true’ when the odd numbered pin (i.e. pin 1) is at logic 1 (-0.8V) and the even numbered pin (i.e. pin 2) is at logic 0 (-1.6V). The typical impedance for twisted pair wire is 100-120 ohms. Differential ECL outputs have 390 ohm pull down resistors to –5.2V. Differential ECL inputs are terminated with 120 ohms. Single ended ECL inputs are terminated with 60 ohms to –2V.