CMC081 Replacement for LeCroy 4300b FERA ADC

Power up as LeCroy 4300b in 11 bit mode.

- 50 ohm input impedance
- gate width 20ns to 500 ns
- Compatible with LeCroy 4300b
- Dead time 8.5 microseconds in Fera mode
- pedestal memory and subtraction
- zero and overflow suppression
- Camac commands and status word as in 4300b
- all other specifications similar to 4300b, whenever possible.

This basic mode is a substitute for the LeCroy 4300b with similar characteristics. This module is not an exact replacement, there are some differences.

- The FERA readout timing is slightly slower. The CMC081 uses an 80 MHz state machine, rather than hard wired ECL logic, to perform the handshakes. The delay from the end of WAK to the next WST is about 40-50 ns.
- The test pulse supplies a DC level (from the DAC input) to the inputs, not a pulse.
- The random Camac data is not cleared by F9
- The full scale and lsb are smaller, 250 pC and 125 fC instead of 500 pC and 250 fC

CMC081 enhancements and added features:

- Built in sliding scale, final DNL <1%.
- Separate sparse readout thresholds independent of pedestal subtraction.
- Two ranges, 8:1, full scale 2 nC or 250 pC.
- Selectable 11 bit or 12 bit mode for each range.
- Improved Fera readout mode.
- FIFO buffers for both Fera and Camac readout.
- Busy output
- Analog Sum output
- Gate Enable / disable
- Four channel mode (0,4,8,12), with reduced dead time (< 4 microseconds)

Gain

Low range, 11 bit mode	125 fC lsb	250 pC fs (power up default)
Low range, 12 bit mode	62 fC lsb	250 pC fs
high range, 11 bit mode	1000 fC lsb	2000 pC fs
high range, 12 bit mode	500 fC lsb	2000 pC fs

High Speed Four channel Mode.

This mode digitizes only 4 of the 16 channels, one from each of the 4 MIQ401 chips. The 16 channels are digitized in the sequence 0,4,8,12,1,5,9,13,2,6,10,14,3,7,11,15. This requires 4 passes through the MIQ chips. The 4 channel mode makes only one pass , digitizing only 0,4,8 and 12. The dead time in this mode is between 3 and 4 microseconds, depending on the readout mode. For example, in uncompressed FERA mode, the REQ line is asserted after 3.5 microseconds.

Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970
tel (845) 364 0211, fax (877) 840 0023, www.cmcamac.com, info@cmcamac.com

CMC081 Front Panel

LEDs

N	lights when module is addressed
A	lights when module is enabled
B	lights when module is Busy

Fera Ecl control bus connector, 8 pair, differential ecl

pair	
1	Not used, connected to ground
2	WST output
3	REQ output
4	CLR input
5	GATE input
6	WAK input
7	GND connected to ground
8	DAC input, 0-10.23 volts (analog)

Behind and between these two connectors is the termination LED. When lighted, it indicates that at least one of the pull down resistor sips is installed.

Fera auxiliary signal connector, 5 pair, differential ecl

Pair	
1	REN input
2	PASS output
3	BUSY output. The BUSY output can be used to control the trigger. It begins at the leading edge of the gate, and ends when the module is cleared (e.g., when an Eclbus CLR is received).
4	ASUM analog sum of all channels on pin 7, pin 8 grounded. The ASUM output can be used in a secondary trigger, or as a monitor. This is an AC coupled, negative signal, the sum of 10% of each input signal
5	Not used, not connected

Signal input Connector, 17 pair, Zin 50 Ohms

Pairs 1-16 Channel 0-15

Pair 17 not used, pins 33 and 34 are connected to ground through 976 Ohm resistors

FeraBus Output Connector, 17 pair, differential ecl

Pairs 1-16 Fera Bus

Pair 17 not used, pins 33 and 34 are connected to ground through 976 Ohm resistors

Note: Differential ecl signals have the odd numbered pin positive true.