CMC080

Sixteen Channel FASTCAMAC Charge Integrating ADC

CE

Firmware Version 23

August 2006

Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970
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CMC080

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General Information

Unpacking and inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the Packing list and damage or shortages reported promptly.

Warranty

Cheesecote Mountain CAMAC warrants its products to operate within specifications under normal use and service for a period of one year from the date of shipment. Replacement parts and repairs are warranted for a period of one year. This warranty extends only to the original purchaser. In exercising this warranty, CMC will repair, or at its option, replace any product returned to us within the warranty period, provided that our examination discloses that the product is defective due to workmanship or materials and has not been damaged by misuse, neglect, accident or abnormal conditions of operation. The purchaser is responsible for the transportation and insurance charges arising from return of products for service. CMC will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, expressed or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. CMC shall not be liable for any special, incidental, or consequential damages, whether in contract or otherwise. CMC products are not designed for use in life support situations or in situations where the operation of the device is essential to assuring health or safety.

Service Procedure

Products requiring maintenance should be returned to CMC. The products returned must be labeled with a Return Authorization Number issued by CMC prior to shipment of the product. All products returned for service must be accompanied by information including the description of the problem and the name, phone number and any other contact information for the user who is returning the product

If under warranty, CMC will repair or replace the product at no charge. The purchaser is only responsible for transportation charges for the return of the product to CMC.

For all products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired. The customer will be billed for the parts and labor for the repair as well as for shipping.

Documentation Discrepancies

CMC is continually improving the quality and performance of its products. Unfortunately, this process can result in documentation that differs in minor details from the products themselves. Where discrepancies arise please be assured that the unit is correct and incorporates the latest modifications to the design.

Contact Information

Questions concerning the installation, calibration and use of this equipment should be directed to Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970, Tel 845 364 0211, fax 877 840 0023. Questions can also be forwarded via Email to info@cmcamac.com. The most current information regarding this product can also be found at www.cmcamac.com

FASTCAMAC Sixteen Channel Charge Integrating ADC Module

- 18 Bit Dynamic Range With 12 Bit Resolution
- 25 fC Per Count On The Most Sensitive Range
- 6,000 pC Full Scale Range Beyond Pedestal
- 10 ns Minimum Gate Period
- Negative Input signals
- 200 mA Peak Input Current
- Fast Clear Input
- Less Than 5.5 μsec Minimum Dead Time
- Sliding Scale for improved DNL
- Pedestal Subtraction
- Sparse Data Scan Mode
- Multi-Event FIFO Buffer
- Normal CAMAC or FASTCAMAC Operation
- CE

For Fast Conversion of Wide Dynamic Range Signals With High Resolution. Designed for High Performance Applications, Including Cherenkov Counters, Fast Scintillation Counters and Calorimeters.

The ADC contains 16 channels of analog-to-digital converter (ADC) with current integrating inputs, 12-bit resolution and 18 bit dynamic range. These negative input gated integrating ADCs can be used to encode fast photo-multiplier and chamber signals or to sample slowly varying signals. The gated integrators are DC-coupled, and are well suited to high rate applications.

This ADC has been designed for short conversion time and maximum data throughput, as required in state-of-the-art physics experiments. The built in data processing can include sliding scale, pedestal subtraction and threshold suppression to (reduce data volume and readout time). The ADC contains a multiple event buffer that can store up to 51 events. Using FASTCAMAC, this buffer can be read out at up to 30 megabytes/sec.

FEATURES

Wide Dynamic Range – The ADC uses the LeCroy Model MQT300A Charge to Time Converter coupled with the LeCroy MTD133b time digitizer to achieve a dynamic range of 18 bits in three overlapping ranges, each with 12 bit resolution.

Narrow Gate Capability- The ADC accepts gate widths between 10 ns and 500 ns.

High Sensitivity – The most sensitive range of the SV080 is 0.025 pC (25 fC) per count, 200 pC full scale. The mid range is 0.2 pC per count, 800 pC full scale. The least sensitive range is 1.5 pC per count, >6 nC full scale.

Built In Auto-ranging – The ADC can be programmed to read all 3 ranges, one selected range, or to auto-range, reading only the correct range (the most sensitive range not overflowed).

Dead Time – The rundown time of the individual ADC is 3.5μsec, followed by the TDC readout time. In auto-range mode the total dead time is less than 5.5 μsec. When all ranges are measured the dead time is less than 8.6 μsec. A selectable 10 bit mode (the rundown is shortened) reduces the dead time to less than 4 μsec.

Fast Clear - In applications where even shorter dead times are required, a fast clear is permitted during the 3 μ sec after the end of the gate (the MQT300a rundown period). When a fast clear is received, the event is aborted and the MQT300a is reset. The dead time ends 1 μsec after the leading edge of the fast clear pulse.

Sliding Scale Mode – A sliding scale can be applied to the MTD133b TDC, effectively averaging the differential non-linearity (DNL) of the TDC over a 16 count range. The resulting DNL is typically too small to be detectable..

Pedestal Subtraction – Individual pedestal values for each channel (and each range, 48 in all) can be subtracted from the data when in auto range mode, resulting in data values directly proportional to the input signal.

Sparse data scan Mode – Individual threshold settings for each channel allow sparse data readout when in auto range mode. The threshold test is applied *after* pedestal subtraction. This will reduce the amount of data stored to the event FIFO, minimizing required readout times.

Multi-event buffer - The ADC includes a FIFO event buffer that holds 19 events when all ranges are measured, and 51 events in auto range mode. The event buffer can be read over CAMAC simultaneously with ADC conversion.

FASTCAMAC readout. The ADC can be read with normal CAMAC or FASTCAMAC crate controllers. Both FASTCAMAC level 1 and level 2 are supported, up to the maximum FASTCAMAC transfer rates. FASTCAMAC Level 1 allows readout at 7.5 Mbytes per second over the CAMAC backplane. FASTCAMAC Level 2 allows readout at up to 30 Mbytes per second. This module is in compliance with FASTCAMAC, DoE/SC-0002

Front Panel Connectors:

Sixteen Lemo cable connectors terminated in 50 Ohms +/- 5%, clamped at +/- 10 V to accept negative input signals.

One Lemo cable connector terminated in 50 Ohms +/- 5% to accept the GATE signal at FAST NIM logic levels

One Lemo cable connector terminated in 50 Ohms +/- 5% to accept the FASTCLEAR signal at FAST NIM logic levels

One Lemo cable connector terminated in 50 Ohms +/- 5% to provide BUSY output at FAST NIM logic levels

Front Panel LED Indicators:

N LED (red) indicates that a CAMAC command is in progress.
B LED (green) indicates that the module is BUSY and unable to accept a gate signal.
D LED (yellow) indicates that at least 1 event is in the FIFO event buffer for readout.

CAMAC Packaging Compatibility: IEEE Std 583, RF-shielded, CAMAC #1

Power Requirements: 2A at +6 V; 2 A at -6 V; 0.45A at +24 V; 0.02A at -24 V.

ORDERING INFORMATION

Contact Cheesecote Mountain Camac, 24 Halley Drive, Pomona, NY 10970
Email: info@cmcamac.com Phone: 845 364 0211 Fax: 845 362 6947

CMC080 Firmware, Version 22 (April 2006)

CAMAC Function Codes implemented:

C, Z	clear everything, data and registers
F0, A0	Read fifo data, no Q if end of event mark, or no event
F0, A1	read control and status register
F0, A2	read FASTCAMAC control register
F0, A3	read event count
F0, A4	read range select register
F0, A5	read firmware version number
F0, A6	read test counter (read counter, read complement and increment)
F1, A0-15	read channel threshold registers
F2, A0-15	read pedestals for low range
F3, A0-15	read pedestals for mid range
F4, A0-15	read pedestals for high range
F5, A0	FASTCAMAC read
F8, A0	test LAM
F9, A0	clear everything, data and registers
F9, A1	clear data only, not registers
F16, A1	write control and status register
F16, A2	write FASTCAMAC control register
F16, A4	write range select register
F17, A0-15	write channel threshold registers
F18, A0-15	write pedestals for low range
F19, A0-15	write pedestals for mid range
F20, A0-15	write pedestals for high range
F24, A0	disable LAM
F24, A1	disable GATE (hold com FF in reset, busy ON)
F26, A0	enable LAM
F26, A1	enable GATE, release com ff reset
F27, A0	test lam enable/disable status
F27, A1	test gate enable/disable status
F27, A2	test BUSY
F27, A3	test if event ready to read
F30, A0	enter programming mode, see below

Register descriptions:

Control Register (24 bits)

bit0(lsb)-7 module ID number (user supplied)
bit8 1 = DC calibration ON, 0 = OFF (default)
bit9-10 operating mode:
0 = read all range data
1 = auto-range mode
2 = not valid
3 = Sparse data mode (auto range, use channel thresholds)
bit11 1 = enable sliding scale
bit12 1 = enable pedestal subtraction (only valid in auto-range and sparse modes)
bit13 1 = add overflow word only if non zero,
0 = always have overflow word
bit14 1 = diagnostic mode, disable sliding scale subtraction
bit15 1 = block mode, read all complete events in buffer
0 = read one event at a time (default)
bit16 1 = 10 bit resolution mode, 4 μsec dead time
0 = 12 bit resolution mode, 5.5 μsec dead time (default)
bit 17 0 = normal Lam, on when any event ready to read (count > 0)
1 = Lam with hysteresis, on when count > 12 (32 in auto range), off count < 6

This register is a 24 bit read/write register and may be used to verify that the CAMAC dataway interface is operational.

FASTCAMAC Control Register (12 bits)

This register follows the FASTCAMAC Control Register and Parameter P specification (version 1.13). the default value for this register is 1, indicating that F5 is a FASTCAMAC level 1 read command.

bit0(lsb)-1 mode, 0 = normal, 1 = level 1, 2 = level 2, 3 = not valid
bit2 0 = leading edge, 1= both edges
bit3 last word Q response, forced to 0 by module (last word is the end of event marker and contains no data)
bit4-5 transfer width, forced to 0, ONLY 24 bit width is implemented
bit6 single (0) or multiple module command (1)
bit7-11 multiple module response order, 0-23

Range Select Register (2 bits)

This register forces the range to the selected range when in AUTO mode. When in sparse mode, the threshold test is performed on the selected range. The default value for this register is 0, which allows normal operation.

bit0(lsb)-1 mode, 0= normal, 1= low range, 2= mid range, 3= hi range

Channel threshold registers (12 bits)

This is the sparse data scan threshold for each channel. The data is stored in the fifo only if the data value for the low range is greater than the threshold value. The data is always stored if the range is high or middle. The 16 registers are 12 bits long (0-11), with bit0 the lsb.

Pedestal subtraction registers

This is the value of the pedestal (unsigned 12 bit integer) to be subtracted from the data values. A pedestal value must be provided for each channel and for each of the three ranges (48 values). The resulting data value (after subtraction) is 14 bits long, and is in twos complement notation. The range of data values is from -8190 to +8191. Note that the data value after pedestal subtraction can be negative.

Event Data Record

The complete record consists of the header, up to 48 data words, and the overflow word that contains overflow flags for all 16 channels. If any channel overflows, there will be no data words for that channel, but there will be a

bit set in the overflow word. If bit 13 in the control register is set, the overflow word will only appear in the event record if there is at least one overflow

Header format (24 bits)

bit0(lsb)-14 copy of control and status register
bit15 don't care, = 0
bit16-19event serial number (also used as delay for sliding scale)
bit20-21don't care, = 0
bit22-23always =2 (identifies header word)

Data word format (24 bits)

bit0(lsb)-13 bits 0-13 are the time data (14 bits) from the MTD
bit14-15bits 14-15 are the range, low=0, mid=1, high=2, 3=overflow
bit16-19bits 16-19 are the channel number
bit20-22don't care, = 0
bit22-23always =0 (identifies data word)

Overflow word format (24 bits)

Bit15-0 overflow flags, =1 if channel is overflowed (no hits in tdc)
Bit16-21 don't care, =0
bit22-23always =3 (identifies overflow word)

Separator word format (24 bits)

Bit21-0 always equal to 00FF hex
bit22-23always =1 (identifies separator word)
This word separates complete events in the FIFO output buffer and is normally accompanied by Q = 0. When in block read mode Q = 1, except after the last event in the block, when Q = 0. This word can always be discarded.

Gate Operation

The gate is a NIM fast level. The pulse length can be as short as 10 ns and as long as 500 ns.

Dead Time

The start for the ADC run down and the common start for the tdc occur at the end of the gate. The total dead time, including the readout of the tdc is less than 5.5 μsec (from the end of the gate) when in auto range or single range mode. In read all range mode the dead time can be up to 1.6 μsec longer (if no ranges are saturated) longer. Busy is asserted during the dead time (and whenever the ADC is not ready for a gate).

Normally, the firmware program uses a 3.5 μS run down for the TDC. This provides the full 12 bits above pedestal. Setting bit 16 in the control register to 1 shortens the run down time to 2 μsec. This results in only 10 bits above pedestal, 1023 counts instead of 4095. The dead time is shorter by 1.5 μS however, only 4 μS instead of 5.5 μS (when in auto-range or single range mode).

Lam Operation

The lam is asserted whenever lam is enabled and there is an event in the fifo buffer, ready to be read out. The lam can only be cleared by reading (or clearing) the data. If Lam hysteresis is selected, the Lam is asserted when the event count is > 12 (32 when in single range or auto range mode) and deasserts when the event count is < 6.

LEDs

The yellow led (B) is lighted by BUSY.
The green led (D) is lighted by the event count greater than zero.
The red led (N) is lighted when the module is addressed (N=1).

Normal CAMAC readout

Normal CAMAC readout is straightforward. If the event count is zero, the f0, A0 command always returns Q=0. If there is an event stored, the first word to be read (a header) is already at the fifo outputs, waiting to be read. The F0, A0 command gates the data out on to the dataway. The last word of the event is the overflow word. Note that the overflow word is present ONLY if one or more of the channels has overflowed.
Q=1 for the header, the data words and the overflow word. The next read after the overflow (if present) is the separator word, and will always return Q=0. If there is another event stored in the fifo, the next read will return the header of that event, with Q=1. In this mode events are read one at a time, with Q=0 between each event.

Block mode CAMAC readout

Block mode CAMAC readout is selected by bit 15 in the control register. If the event count is zero, the f0, A0 command always returns Q=0. If there is an event stored, the first word to be read (a header) is already at the fifo outputs, waiting to be read. The F0, A0 command gates the data out on to the dataway. The last word of the event is the overflow word. Note that the overflow word is present ONLY if one or more of the channels has overflowed.
Q=1 for the header, the data words and the overflow word. The next read after the overflow (if present) is the separator word. In Block mode, if there is another event in the buffer waiting to be read, Q=1. If there are no more complete events in the FIFO, Q=0.

FASTCAMAC readout

FASTCAMAC readout is similar to normal CAMAC, both single event and block mode transfers are implemented. Only 24 bit read transfers are implemented. There are no 48 bit reads, and no FASTCAMAC writes. Level 1 allows transfers at up to 7.5 Mbytes/sec. Level 2 can operate at the maximum rate of 100 ns per transfer, or 30 Mbytes/sec (both S1 edges are used to transfer data), or any other allowed FASTCAMAC rate, either single edge or double edge. Multiple module transfers are also implemented, for both level 1 and level 2. All FASTCAMAC commands use F5, A0. The FASTCAMAC options are selected by writing to the FASTCAMAC control register.

Basic Operation

The minimum necessary to operate the module after power up is to clear everything (F9, A0) and enable the GATE (F26, A1). This will give basic multi-range mode with all ranges read out, and the sliding scale disabled. This will result in 50 data words for each GATE. To reduce the record size, use the control register (F16, A1) to select multi-range mode (control register bit 9, = 512) or select a single range with the range select register (F16, A4). Also select overflow word only if not zero (control register bit 13, = 8192). This will reduce the data record to 17 words. If not all channels are needed, disable individual channels by selecting sparse mode, and setting the channel thresholds to 0 for each channel in use, and to 4095 for each channel to be disabled. The data record will be reduced to one (the header) plus the number of channels in use.

Reloading the FPGA program from the EEPROM

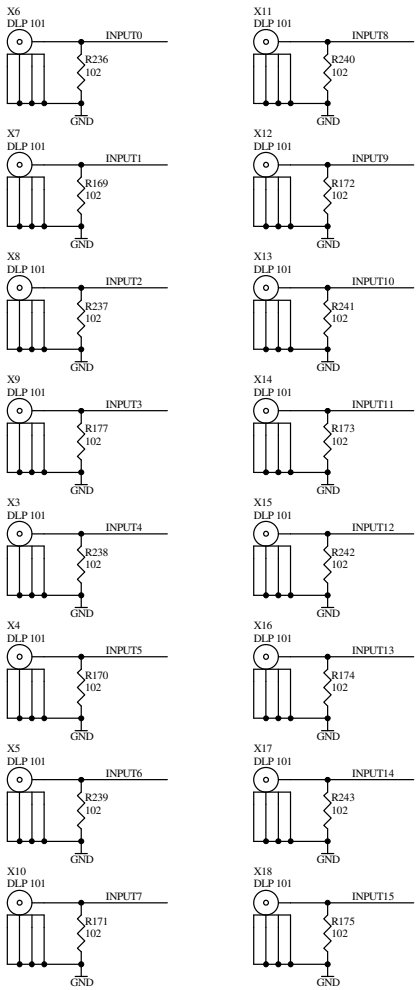
All of the sequencing and control logic is implemented in the Xilinx 4013 FPGA. The FPGA is RAM based, and must be reloaded each time that power is applied. This is normally transparent to the user, and a few hundred milliseconds after power is applied, the FPGA is ready to use.
The flash memory chip is large enough to store two complete programs for the FPGA, the normal program, and an alternate program. To load the alternate program, follow this sequence of CAMAC instructions.

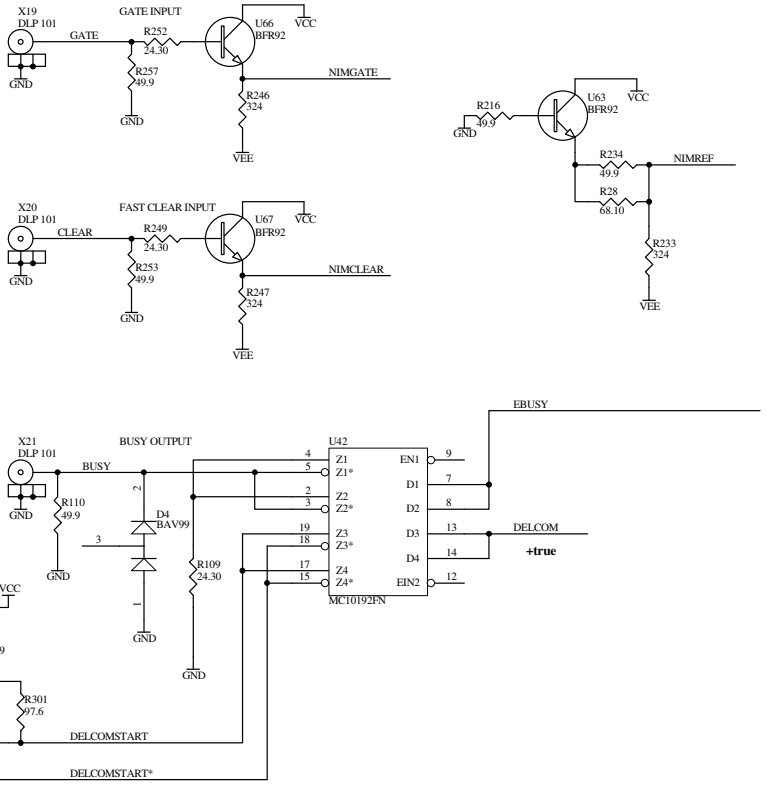
F30, A0	this enables the FPGA programming mode, with the normal program selected. The FPGA is cleared and a limited set of CAMAC commands are available.
F21, A0	this selects the alternate program, omit this step to reload the normal program
F25, A0	begin programming from the selected part of the EEPROM
F14, A0	test FPGA INIT line, Loop on this command until Q = 1
F13, A0	test FPGA DONE line. Loop on this command until Q = 1
F9, A0	exit programming mode. The special instructions are disabled, except for F30, A0. The CAMAC commands programmed into the FPGA are now operational.

The normal program is the current version. The alternate program is the same. This feature is reserved for future enhancements that may not be compatible with the normal firmware program.

The flash memory chip is in a socket. This allows simple field updates of the firmware by replacing the chip. Firmware updates, when available will be offered at no charge.

Schematics

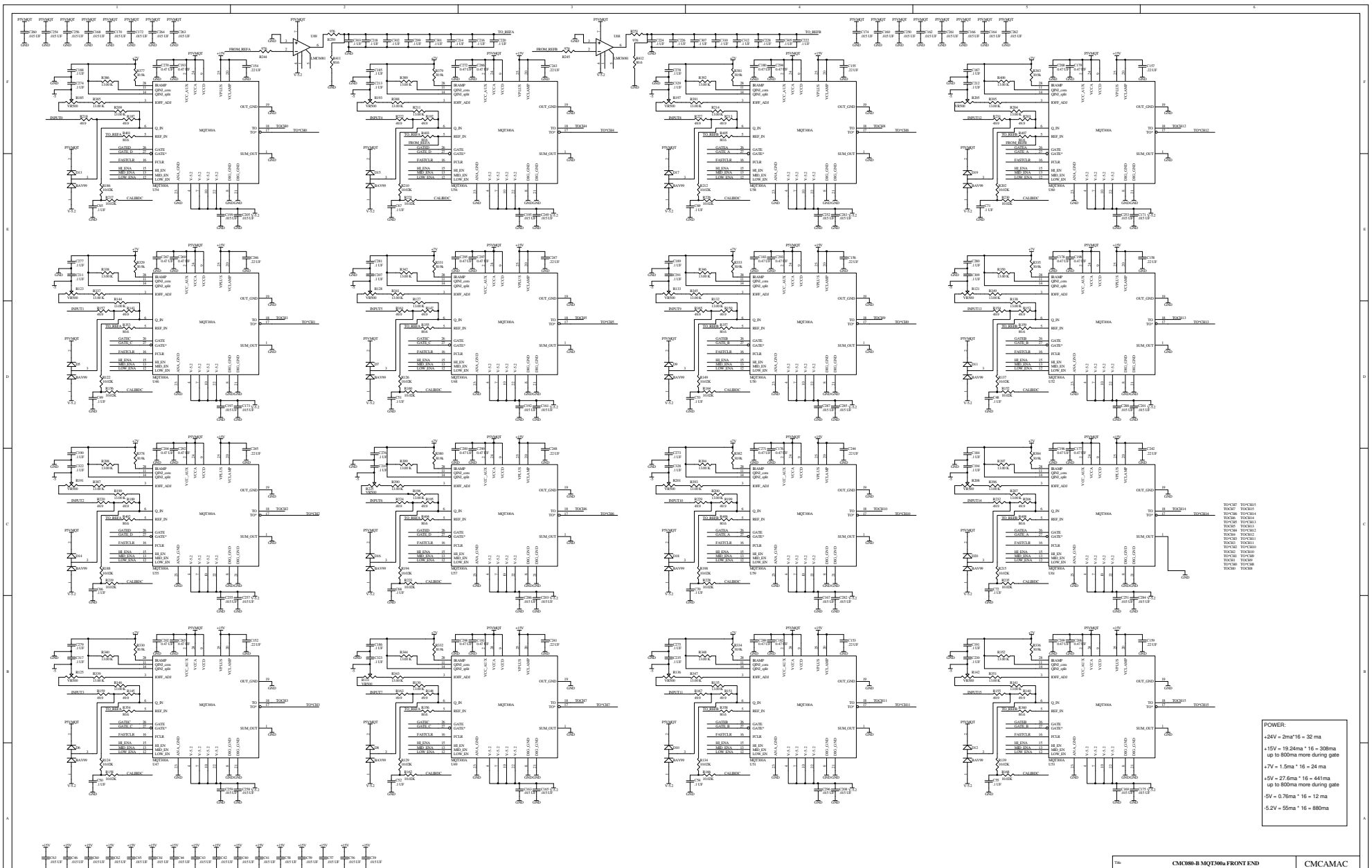


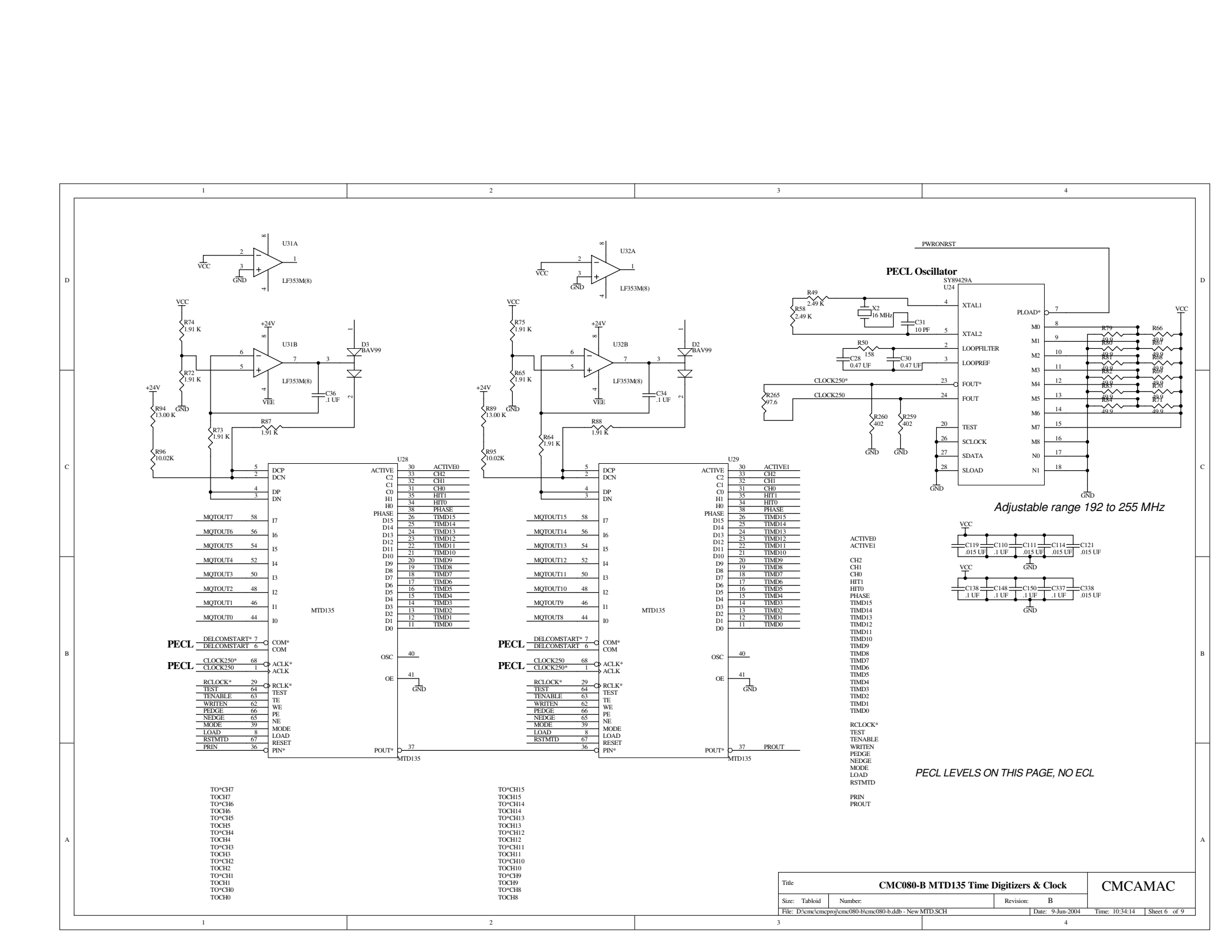


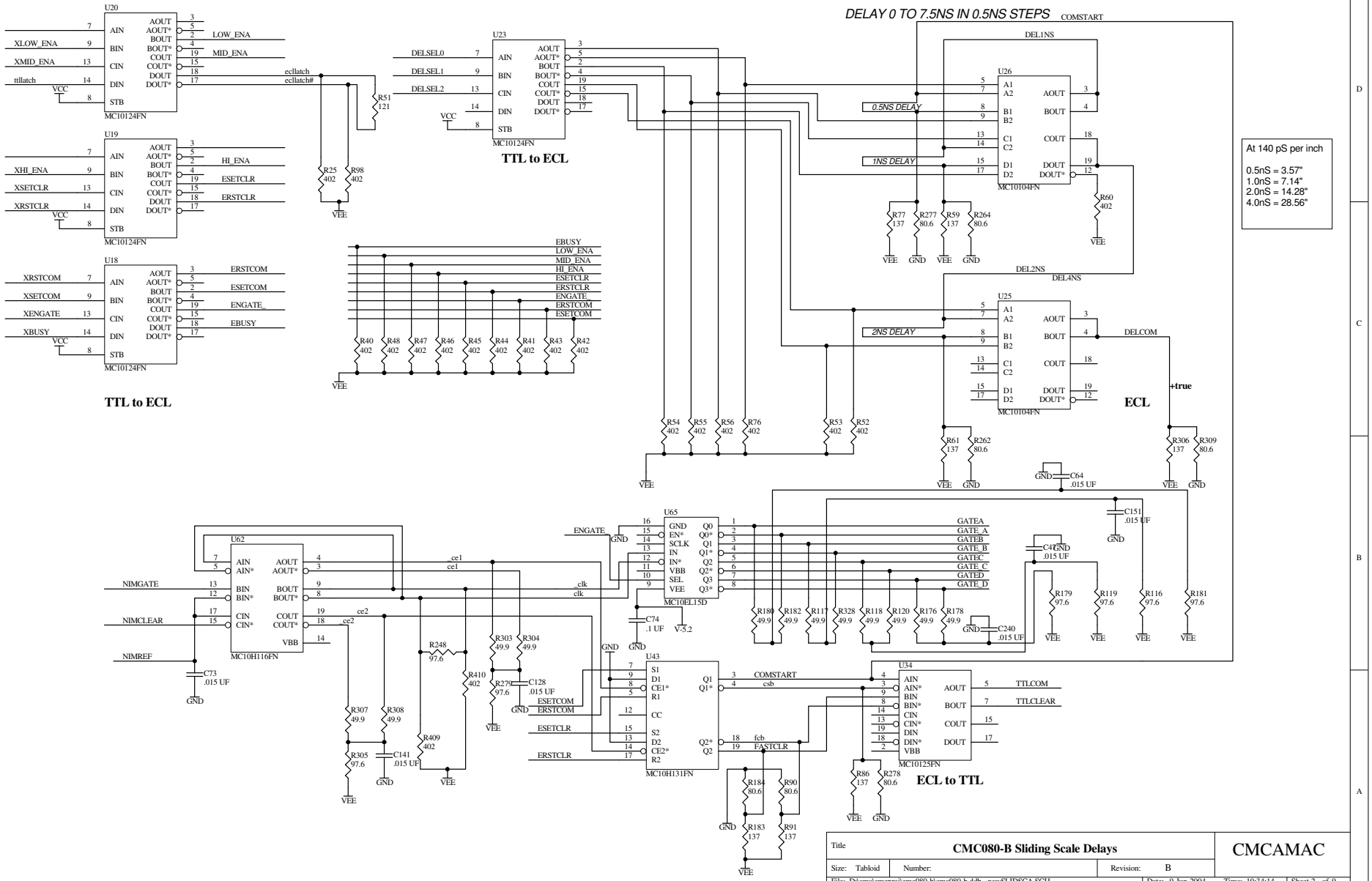
ecl to pecl

COM is PECL, not ECL

Title	**CMC080-B Inputs**		CMCAMAC
Size: Tabloid	Number:	Revision: B	
File: D:\cmc\cmcproj\cmc080-b\cmc080-b.ddb - newINPUTS.SCH		Date: 9-Jun-2004	Time: 10:34:13 Sheet 8 of 9


MQT300A
LMC6081
TO_REFA
TO_REFB
FROM_REFA
FROM_REFB
POWER:
+24V = 2ma*16 = 32 ma
+15V = 19.24ma * 16 = 308ma
up to 800ma more during gate
+7V = 1.5ma * 16 = 24 ma
+5V = 27.6ma * 16 = 441ma
up to 800ma more during gate
-5V = 0.76ma * 16 = 12 ma
-5.2V = 55ma * 16 = 880ma
CMCAMAC
CMC080-B MQT300a FRONT END
Number:
Revision: B
Date: 9-Jan-2009
Sheet 2 of 9


U31A
LF353M(8)
U32A
LF353M(8)
PECL Oscillator
SY89429A
U24
Adjustable range 192 to 255 MHz
U31B
U32B
U28
U29
MTD135
PECL
PECL LEVELS ON THIS PAGE, NO ECL
CMC080-B MTD135 Time Digitizers & Clock
CMCAMAC
Size: Tabloid
Number:
Revision: B
File: D:\cmc\cmcproj\cmc080-b\cmc080-b.ddb - New MTD.SCH
Date: 9-Jun-2004
Time: 10:34:14
Sheet 6 of 9


DELAY 0 TO 7.5NS IN 0.5NS STEPS
COMSTART
DEL1NS
DEL2NS
DEL4NS
0.5NS DELAY
1NS DELAY
2NS DELAY
DELCOM
+true
ECL
TTL to ECL
TTL to ECL
ECL to TTL
U20
U19
U18
U23
U26
U25
U62
U65
U43
U34
MC10124FN
MC10104FN
MC10H116FN
MC10EL15D
MC10H131FN
MC10125FN
LOW_ENA
MID_ENA
HI_ENA
ESETCLR
ERSTCLR
ENGATE_
EBUSY
ERSTCOM
ESETCOM
ecllatch
ecllatch#
XLOW_ENA
XMID_ENA
ttllatch
XHI_ENA
XSETCLR
XRSTCLR
XSETCOM
XENGATE
XBUSY
DELSEL0
DELSEL1
DELSEL2
NIMGATE
NIMCLEAR
NIMREF
ENGATE
GATEA
GATE_A
GATEB
GATE_B
GATEC
GATE_C
GATED
GATE_D
COMSTART
csb
FASTCLR
fcb
TTLCOM
TTLCLEAR
_ce1
ce1
ce2
_clk
clk
ESETCOM
ERSTCOM
ESETCLR
ERSTCLR
At 140 pS per inch
0.5nS = 3.57"
1.0nS = 7.14"
2.0nS = 14.28"
4.0nS = 28.56"
CMC080-B Sliding Scale Delays
CMCAMAC
Size: Tabloid
Number:
Revision: B
File: D:\cmc\cmcproj\cmc080-b\cmc080-b.ddb - newSLIDSCA.SCH
Date: 9-Jun-2004
Time: 10:34:14
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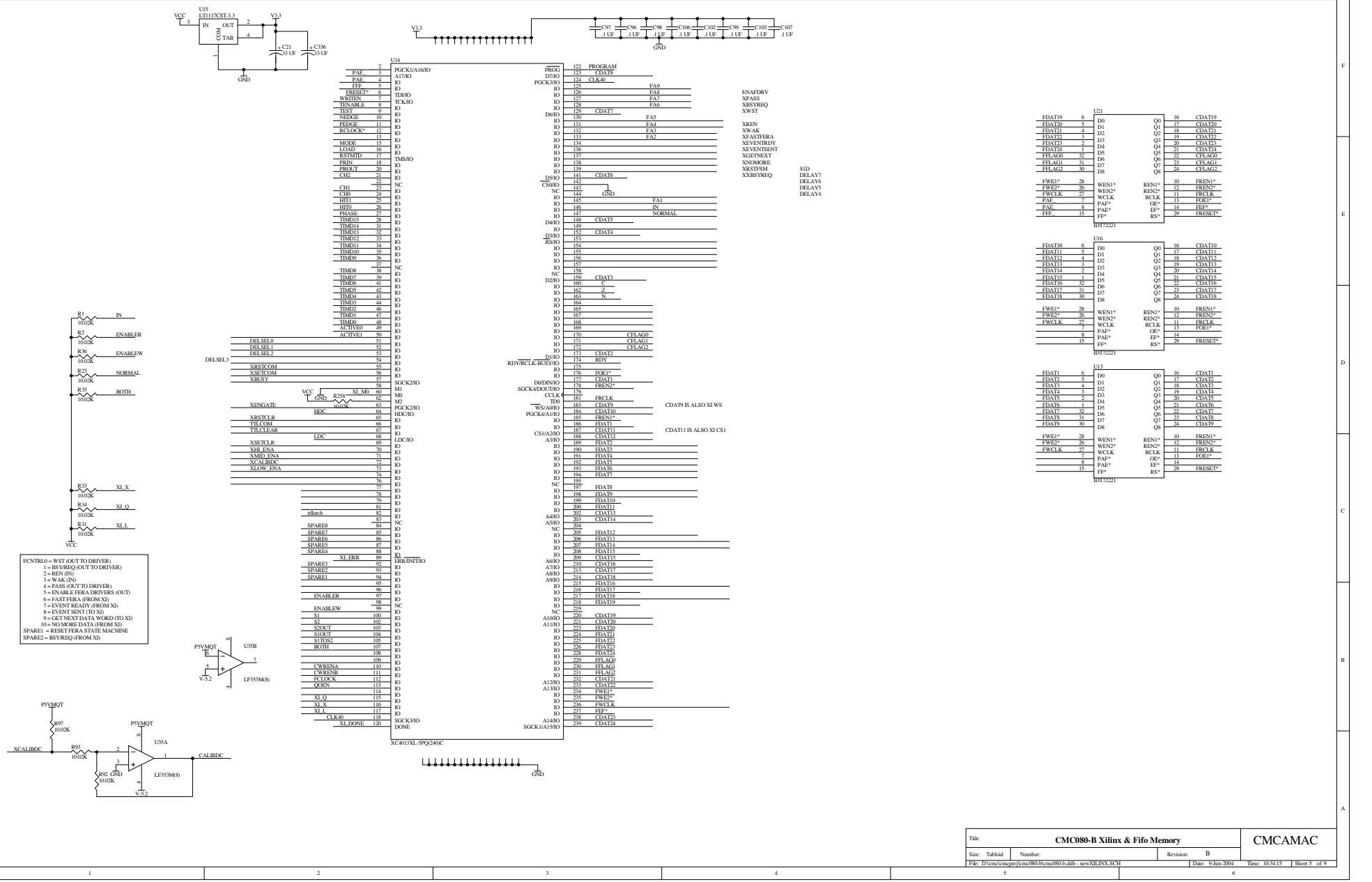
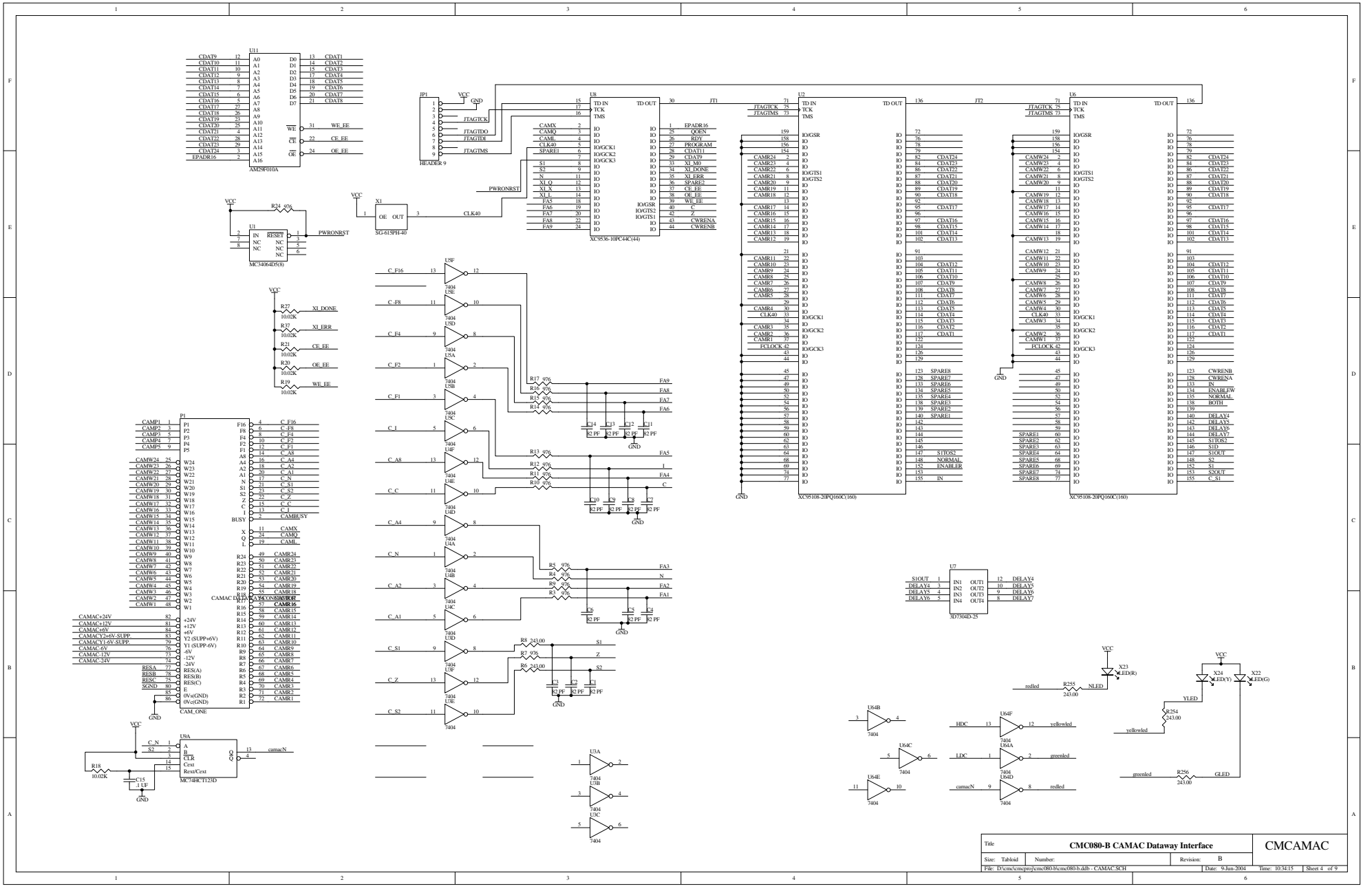
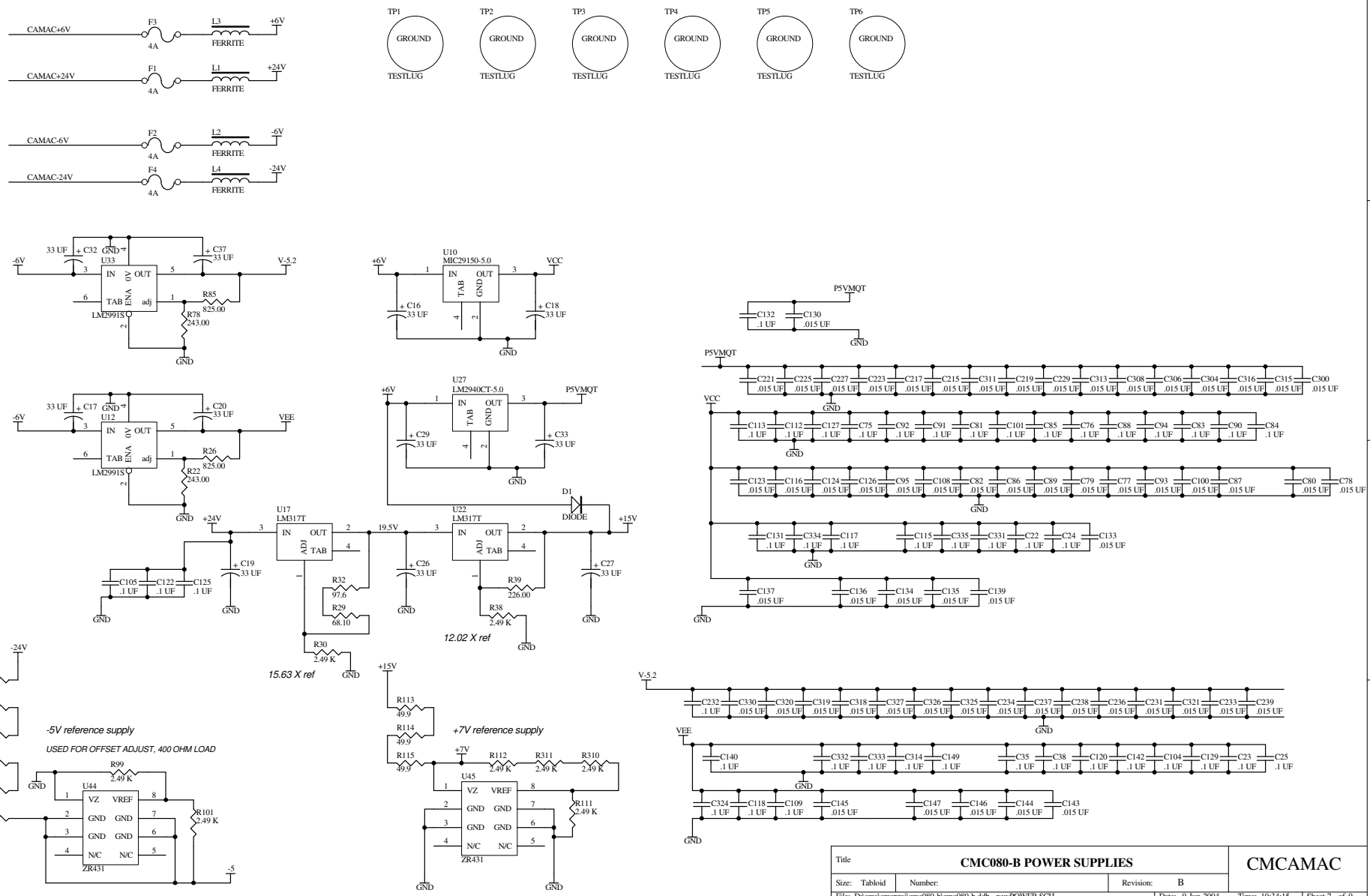


Title	**CMC080-B Xilinx & Fifo Memory**
Size: Tabloid	Number:
Revision:	B
File: D:\cmc\cmcpro\cmc080-b\cmc080-b.ddb - newXILINX.SCH	Date: 9-Jun-2004
Time: 10:34:15	Sheet 5 of 9
CMCAMAC	



Title	**CMC080-B CAMAC Dataway Interface**		CMCAMAC
Size: Tabloid	Number:	Revision: B	
File: D:\cmc\cmcpro\jcmc080-b\cmc080-b.ddb - CAMAC.SCH		Date: 9-Jun-2004	Time: 10:34:15 Sheet 4 of 9


CAMAC+6V
F3
4A
L3
FERRITE
+6V
CAMAC+24V
F1
4A
L1
FERRITE
+24V
CAMAC-6V
F2
4A
L2
FERRITE
-6V
CAMAC-24V
F4
4A
L4
FERRITE
-24V
TP1
GROUND
TESTLUG
TP2
GROUND
TESTLUG
TP3
GROUND
TESTLUG
TP4
GROUND
TESTLUG
TP5
GROUND
TESTLUG
TP6
GROUND
TESTLUG
-6V
33 UF
C32
GND
U33
LM2991S
IN
0V
OUT
TAB
ENA
adj
C37
33 UF
V-5.2
R85
825.00
R78
243.00
GND
+6V
U10
MIC29150-5.0
IN
OUT
TAB
GND
VCC
C16
33 UF
C18
33 UF
GND
-6V
33 UF
C17
GND
U12
LM2991S
C20
33 UF
VEE
R26
825.00
R22
243.00
GND
+6V
U27
LM2940CT-5.0
P5VMQT
C29
33 UF
C33
33 UF
GND
D1
DIODE
+24V
U17
LM317T
IN
OUT
ADJ
TAB
19.5V
U22
LM317T
+15V
C105
.1 UF
C122
.1 UF
C125
.1 UF
C19
33 UF
GND
R32
97.6
R29
68.10
R30
2.49 K
15.63 X ref
C26
33 UF
R39
226.00
R38
2.49 K
12.02 X ref
C27
33 UF
P5VMQT
C132
.1 UF
C130
.015 UF
GND
C221
.015 UF
C225
.015 UF
C227
.015 UF
C223
.015 UF
C217
.015 UF
C215
.015 UF
C311
.015 UF
C219
.015 UF
C229
.015 UF
C313
.015 UF
C308
.015 UF
C306
.015 UF
C304
.015 UF
C316
.015 UF
C315
.015 UF
C300
.015 UF
VCC
C113
.1 UF
C112
.1 UF
C127
.1 UF
C75
.1 UF
C92
.1 UF
C91
.1 UF
C81
.1 UF
C101
.1 UF
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.1 UF
C76
.1 UF
C88
.1 UF
C94
.1 UF
C83
.1 UF
C90
.1 UF
C84
.1 UF
C123
.015 UF
C116
.015 UF
C124
.015 UF
C126
.015 UF
C95
.015 UF
C108
.015 UF
C82
.015 UF
C86
.015 UF
C89
.015 UF
C79
.015 UF
C77
.015 UF
C93
.015 UF
C100
.015 UF
C87
.015 UF
C80
.015 UF
C78
.015 UF
C131
.1 UF
C334
.1 UF
C117
.1 UF
C115
.1 UF
C335
.1 UF
C331
.1 UF
C22
.1 UF
C24
.1 UF
C133
.015 UF
C137
.015 UF
C136
.015 UF
C134
.015 UF
C135
.015 UF
C139
.015 UF
V-5.2
C232
.1 UF
C330
.015 UF
C320
.015 UF
C319
.015 UF
C318
.015 UF
C327
.015 UF
C326
.015 UF
C325
.015 UF
C234
.015 UF
C237
.015 UF
C238
.015 UF
C236
.015 UF
C231
.015 UF
C321
.015 UF
C233
.015 UF
C239
.015 UF
VEE
C140
.1 UF
C332
.1 UF
C333
.1 UF
C314
.1 UF
C149
.1 UF
C35
.1 UF
C38
.1 UF
C120
.1 UF
C142
.1 UF
C104
.1 UF
C129
.1 UF
C23
.1 UF
C25
.1 UF
C324
.1 UF
C118
.1 UF
C109
.1 UF
C145
.015 UF
C147
.015 UF
C146
.015 UF
C144
.015 UF
C143
.015 UF
-24V
R103
158
R106
158
R108
158
R107
158
R105
158
R102
158
-5V reference supply
USED FOR OFFSET ADJUST, 400 OHM LOAD
R99
2.49 K
U44
ZR431
VZ
VREF
GND
N/C
R101
2.49 K
-5
+15V
R113
49.9
R114
49.9
R115
49.9
+7V reference supply
+7V
R112
2.49 K
R311
2.49 K
R310
2.49 K
U45
ZR431
R111
2.49 K
Title
CMC080-B POWER SUPPLIES
CMCAMAC
Size: Tabloid
Number:
Revision: B
File: D:\cmc\cmcproj\cmc080-b\cmc080-b.ddb - newPOWER.SCH
Date: 9-Jun-2004
Time: 10:34:15
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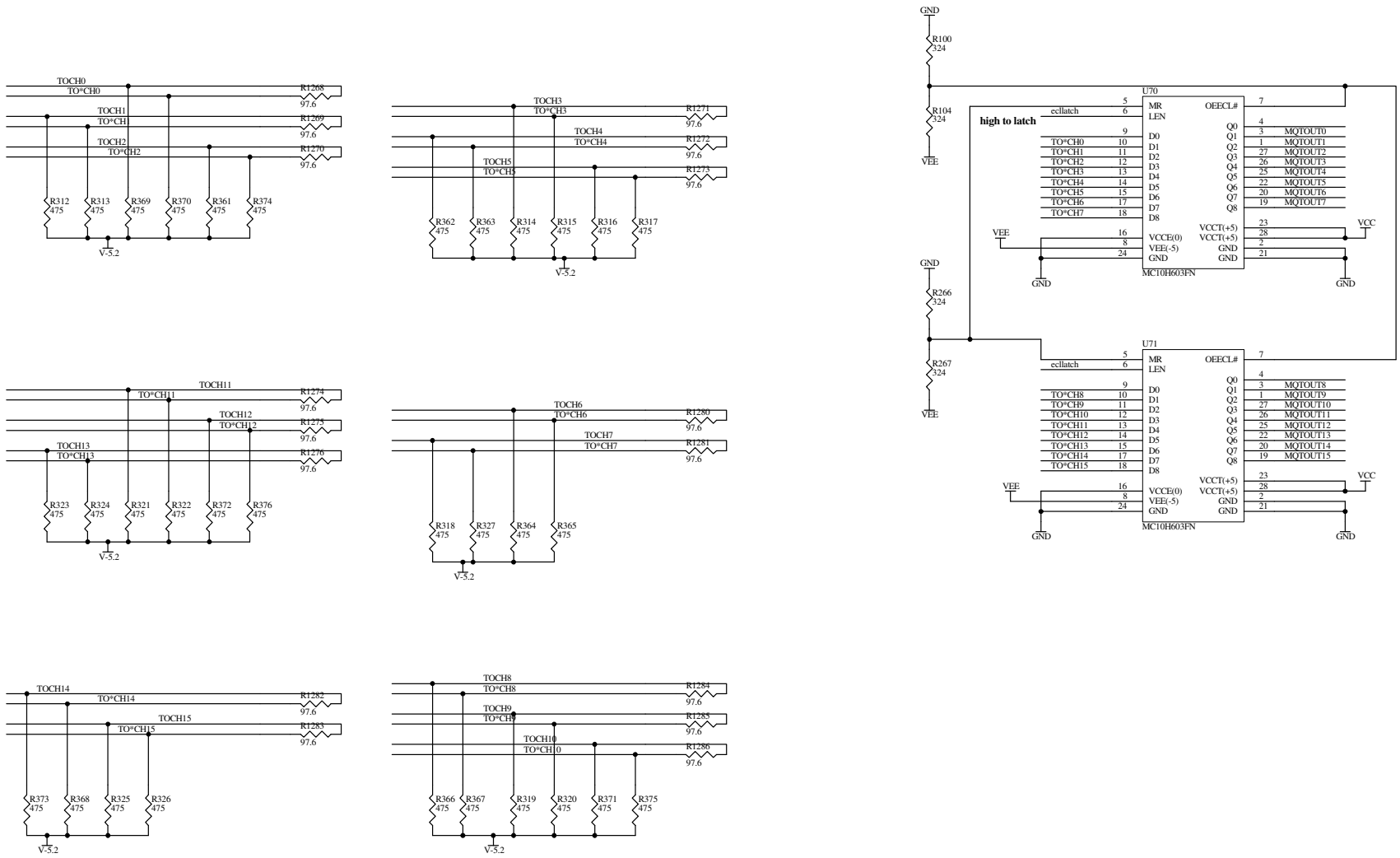

Title	**CMC080-B Level Shifters**		CMCAMAC
Size: Tabloid	Number:	Revision: B	
File: D:\cmc\cmcproj\cmc080-b\cmc080-b.ddb - newLEVELShifters.sch		Date: 9-Jun-2004	Time: 10:34:15 Sheet 7 of 9