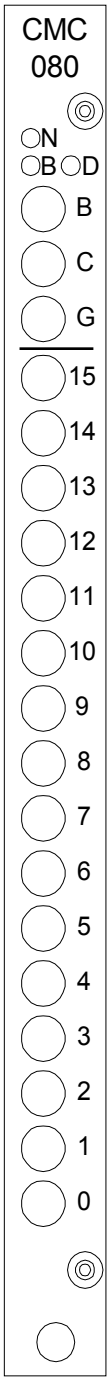
CMC080 *FAST*CAMAC 16 Channel Charge Integrating ADC

- 18 Bit Dynamic Range With 12 Bit Resolution
- 25 fC Per Count On The Most Sensitive Range
- 6,000 pC Full Scale Range Beyond Pedestal
- 10 ns Minimum Gate Period
- Negative Input signals
- 200 mA Peak Input Current
- Fast Clear Input
- Less Than 5.5 μsec Minimum Dead Time
- Sliding Scale for improved DNL
- Pedestal Subtraction
- Sparse Data Scan Mode
- Multi-Event FIFO Buffer
- Normal CAMAC or FASTCAMAC Operation, Level 1 & Level 2
- CE



For Fast Conversion of Wide Dynamic Range Signals With High Resolution. Designed for High Performance Applications, Including Cherenkov Counters, Fast Scintillation Counters and Calorimeters.

The ADC contains 16 channels of analog-to-digital converter (ADC) with current integrating inputs, 12-bit resolution and 18 bit dynamic range. These negative input gated integrating ADCs can be used to encode fast photo-multiplier and chamber signals or to sample slowly varying signals. The gated integrators are DC-coupled, and are well suited to high rate applications.

This ADC has been designed for short conversion time and maximum data throughput, as required in state-of-the-art physics experiments. The built in data processing can include sliding scale, pedestal subtraction and threshold suppression to (reduce data volume and readout time). The ADC contains a multiple event buffer that can store up to 51 events. Using FASTCAMAC, this buffer can be read out at up to 30 megabytes/sec.

FEATURES

Wide Dynamic Range – The ADC uses the LeCroy Model MQT300A Charge to Time Converter coupled with the LeCroy MTD133b time digitizer to achieve a dynamic range of 18 bits in three overlapping ranges, each with 12 bit resolution.

Narrow Gate Capability- The ADC accepts gate widths between 10 ns and 500 ns.

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High Sensitivity – The most sensitive range of the SV080 is 0.025 pC (25 fC) per count, 200 pC full scale. The mid range is 0.2 pC per count, 800 pC full scale. The least sensitive range is 1.5 pC per count, >6 nC full scale.

Built In Auto-ranging – The ADC can be programmed to read all 3 ranges, one selected range, or to auto-range, reading only the correct range (the most sensitive range not overflowed).

Dead Time – The rundown time of the individual ADC is 3.5μsec, followed by the TDC readout time. In auto-range mode the total dead time is less than 5.5 μsec. When all ranges are measured the dead time is less than 8.6 μsec. A selectable 10 bit mode (the rundown is shortened) reduces the dead time to less than 4 μsec.

Fast Clear - In applications where even shorter dead times are required, a fast clear is permitted during the 3 μsec after the end of the gate (the MQT300a rundown period). When a fast clear is received, the event is aborted and the MQT300a is reset. The dead time ends 1 μsec after the leading edge of the fast clear pulse.

Sliding Scale Mode – A sliding scale can be applied to the MTD133b TDC, effectively averaging the differential non-linearity (DNL) of the TDC over a 16 count range. The resulting DNL is typically too low to measure

Pedestal Subtraction – Individual pedestal values for each channel (and each range, 48 in all) can be subtracted from the data when in auto range mode, resulting in data values directly proportional to the input signal.

Sparse data scan Mode – Individual threshold settings for each channel allow sparse data readout when in auto range mode. The threshold test is applied *after* pedestal subtraction. This will reduce the amount of data stored to the event FIFO, minimizing required readout times.

Multi-event buffer - The ADC includes a FIFO event buffer that holds 19 events when all ranges are measured, and 51 events in auto range mode. The event buffer can be read over CAMAC simultaneously with ADC conversion.

FASTCAMAC readout. The ADC can be read with normal CAMAC or FASTCAMAC crate controllers. Both FASTCAMAC level 1 and level 2 are supported, up to the maximum FASTCAMAC transfer rates. FASTCAMAC Level 1 allows readout at 7.5 Mbytes per second over the CAMAC backplane. FASTCAMAC Level 2 allows readout at up to 30 Mbytes per second. This module is in compliance with FASTCAMAC, DoE/SC-0002

Front Panel Connectors:

Sixteen Lemo cable connectors terminated in 50 Ohms +/- 5%, clamped at +/- 10 V to accept negative input signals.

One Lemo cable connector terminated in 50 Ohms ± 5% to accept the GATE signal at FAST NIM logic levels

One Lemo cable connector terminated in 50 Ohms ±5% to accept the CLEAR signal.at FAST NIM logic levels

One Lemo cable connector terminated in 50 Ohms ±% to provide BUSY output at FAST NIM logic levels

Front Panel LED Indicators:

N LED (red) indicates that a CAMAC command is in progress.
B LED (green) indicates that the module is BUSY and unable to accept a gate signal.
D LED (yellow) indicates that at least 1 event is in the FIFO event buffer for readout.

CAMAC Packaging Compatibility: IEEE Std 583, RF-shielded, CAMAC #1

Power Requirements: 2A at +6 V; 2 A at -6 V; 0.45A at +24 V; 0.02A at -24 V.